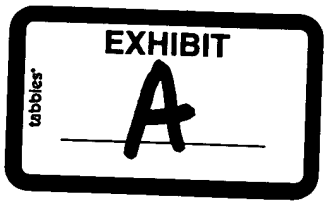
#5
12-10-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Manpreet S. Khaira et al.	Examiner:	Samarina Makhdoom
Serial No.:	09/347,690	Group Art Unit:	2123
Filed:	July 2, 1999	Docket:	884.107US1
Title:	LOGIC VERIFICATION IN LARGE SYSTEMS		

DECLARATION UNDER 37 C.F.R. § 1.131



Commissioner for Patents
Washington, D.C. 20231

This declaration is submitted under 37 C.F.R. § 1.131 prior to any final rejection of U.S. Patent Application Serial Number 09/347,690 to establish invention of the subject matter of the rejected claims prior to the effective date of the reference authored by Casas, et al. "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding of VLSI Design, Jan. 7-10, 1999 (hereinafter "Casas"), on which the rejections are based.

I, Jeremy S. Casas, do hereby declare:

1. On July 2, 1999, the filing date of the Application designated above (hereinafter the "Application"), I was an employee of Intel Corporation, the assignee of the Application.
2. I am a joint inventor of all claims of the present application.
3. Prior to the year 1999, I conceived the inventive subject matter in the United States as evidenced by a copy of a signed invention disclosure form attached hereto as Exhibit I and diligently worked to constructively reduce the inventive subject matter to practice as evidenced by the filing of the Application for the claimed embodiments of the invention. I worked with a patent attorney as my other duties permitted in preparing the Application for filing with the United States Patent and Trademark Office. On information and belief, I received at least one draft of the Application for review and revision on or about May 4, 1999.
4. The dates redacted from Exhibit I are prior to the year 1999.
5. Other material redacted from Exhibit I is not related to dating the conception or reduction to practice of the inventive subject matter.

6. Tom Tetzlaff was not an inventor of the inventive subject matter. Mr. Tetzlaff worked as an intern at Intel Corporation, and was directed to create programs which operated according to various embodiments of the invention after it was conceived. Mr. Tetzlaff worked as a programmer under my supervision, and the supervision of Honghua Yang.

8. The patent application was filed on July 2, 1999.

9. The invention was completed by me as the co-inventor of the subject matter of claims under rejection.

10. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: NOV. 20, 2002

Jeremy S. Casas

Respectfully submitted,
MANPREET S. KHAIRA ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2103

Date November 27, 2002 By Danny Padys
Danny J. Padys
Reg. No. 35,635

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 27 day of November, 2002.

Name Jane Sugers

Signature Jane Sugers

EXHIBIT I

REDACTED INVENTION DISCLOSURE FORM

INTEL CONFIDENTIAL

FOR ML IP COMMITTEE

(ML Comm)

INTEL INVENTION DISCLOSURE

MPG/DT/SCL

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Inventor: Khaira (Last Name) Manpreet (First Name)
SS# 161-70-1145 WWID 10059521 Phone 503-264-9316 M/S: JFT-102
Home Address: 5245 NW 152nd St City Portland State OR Zip 97229
Citizenship: Indian BUM Presenter:
Group: (e.g. TMG, ICG, CEG) MPG Division Name DT Subdivision SCL
Supervisor* Gadi Singer WWID 10010703 Phone 4-865-6168 M/S: IDC-4C

Inventor: Otto (Last Name) Steve (First Name) W (Middle Initial)
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Inventor: Yang (Last Name) Honghua (First Name) H (Middle Initial)
SS# 644-07-4125 WWID 10073990 Phone 503-264-2973 M/S: JFT-102
Home Address: 14430 NW Whistler Ln City Portland State OR Zip 97229
Citizenship: Chinese BUM Presenter:
Group: (e.g. TMG, ICG, CEG) MPG Division Name DT Subdivision SCL
Supervisor* Naveed Sherwani WWID 10073659 Phone 503-264-1238 M/S: JFT-102

Inventor: Joshi (Last Name) Mandar (First Name) S (Middle Initial)
SS# 628-01-6667 WWID 10060018 Phone 503-264-4044 M/S: JFT-102
Home Address: 268 SW 212th Ave City Aloha State OR Zip 97006
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Inventor: Seligman (Last Name) Erik (First Name) M (Middle Initial)

SS# 137-60-3449 WWID 10068627 Phone 503-264-2590 M/S: JFT-102

Home Address: 1885 NW Rolling Hill Dr City Beaverton State OR Zip 97006

Citizenship: USA BUM Presenter:

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Supervisor* Steve Otto WWID 10073620 Phone 503-264-2592 M/S: JFT-102

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Simulation of Large Circuits on Intel Servers

3. What technology/product/process (code name) does it relate to: _ Circuit Logic Verification

4. Stage of development (i.e. % complete) 100%

5. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

NO: X YES: DATE WAS OR WILL BE PUBLISHED:

If YES, was the manuscript submitted for pre-publication approval? YES: NO:

(b) Has your invention been used/sold or planned to be used/sold by Intel or others? (In use at Intel)

NO: YES: X DATE WAS OR WILL BE SOLD: None

(c) *Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?*

NO: X YES: Name of SIG/Standard/Specification:

(d) If the invention is a semiconductor device, actual or anticipated date of tapeout?

(e) If the invention is software, actual or anticipated date of any beta tests. _ already in use

6. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia?

NO: X YES: Name of individual or entity:

PLEASE READ AND FOLLOW THE DIRECTIONS ON THE ATTACHED PAGE ON HOW TO WRITE A DESCRIPTION OF YOUR INVENTION

Please attach a page to this form, *DATED AND SIGNED BY AT LEAST ONE PERSON WHO* IS NOT A NAMED INVENTOR, to provide a description of the invention, and include the following information:

1. Describe in detail how the invention works.
2. Describe advantage(s) of your invention over what is done now.
3. Include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.
4. Value of your invention to Intel (how will it be used?).
5. Identify the closest or most pertinent prior art that you are aware of.
6. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

*HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM

[redacted] Navneet S. Khan [redacted]

GREG SPIRAKIS

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

SIMULATION OF LARGE CIRCUITS ON INTEL SERVERS

Manpreet Khaira, Steve Otto, Honghua Hannah Yang, Mandar Joshi, Jeremy Casas, Erik Seligman

MS-JFT-104 {hyang, jcasas}@ichips.intel.com

INVENTION AND HOW IT WORKS

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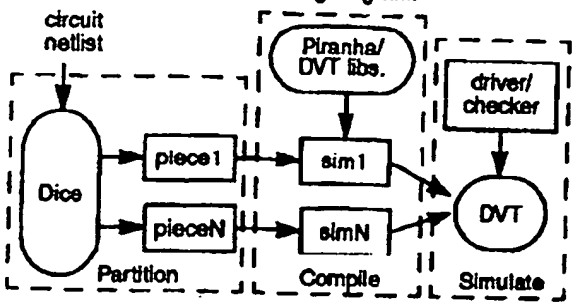

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- Dice partitioner has the use of a combination of several powerful activity weight functions in the load balance scheme. They cover all types of devices in micro-processor designs such as multiple clocks, and non-latch sequential elements.

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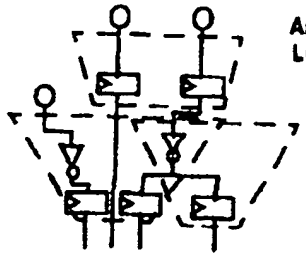
(1) A circuit partitioner based on a new idea called "extended Latch Boundary Component decomposition", or extended LBCs. The LBC concept by itself is not new. Innovation in our partitioner is to determine how to cluster the LBCs to form extended LBCs, so that the overall simulation speeds up. An extended LBC is a subcircuit that starts from latches and/or primary outputs and ends at latches and/or primary inputs. An extended LBC may contain internal latches and may overlap with another LBC. Dice decomposes a circuit into extended LBCs by traversing the circuit hierarchy and putting heavily correlated devices into the same extended LBC so as to reduce logic replication and reduce the final communication cost.



Our extended LBC formulation : only 2 communication steps are needed to evaluate the circuit every clock phase. We are also able to minimize circuit replication to about 10%, and communication cost to less than 10% of the total time.

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This scheme is independent of latches. In addition, it handles multiple clocks, since elements connecting to slow clocks have low activity. It also handles other sequential elements such as memory devices and state holders that are not latches.

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We use a broadcast-and-collect algorithm which *substantially improves performance* by removing the time to process data packets arriving.

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Technical Witness: TIMOTHY KAM

Timothy Kam

The Shark approach to solving switch-level circuit simulation makes it the solution for all future Intel logic verification (LVR) needs. It will save dollars by eliminating the need to purchase custom hardware accelerators

From a throughput perspective, Shark runs on standard workstations. This allows designers to do LVR on their designs whenever they want to and not wait in line on a few hardware accelerators as was done previously. This should help increase the quality of the processor (by running more tests due to availability of compute cycles) and at the same time increase the productivity of the designers by eliminating wait-time on LVR runs.

Currently, Shark is the tool-of-choice for performing LVR of current processor design groups and will most likely be used by all future processor design groups. It is also being evaluated by other chip design teams . In fact, we don't expect to be buying any more hardware accelerators for logic verification.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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I, Honghua H. Yang, do hereby declare:

1. On July 2, 1999, the filing date of the Application designated above (hereinafter the "Application"), I was an employee of Intel Corporation, the assignee of the Application.
2. I am a joint inventor of all claims of the present application.
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Date: 11/20/2002

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MANPREET S. KHAIRA ET AL.

By their Representatives,

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P.O. Box 2938
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(612) 371-2103

Date November 27, 2002 By Danny Padys
Danny I. Padys
Reg. No. 35,635

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Name Jane Sagers

Signature Jane Sagers

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Inventor: Seligman (Last Name) Erik (First Name) M (Middle Initial)

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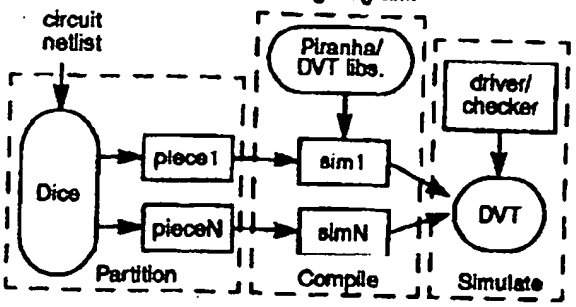

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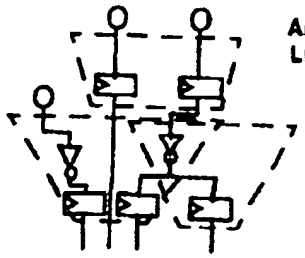

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1. On July 2, 1999, the filing date of the Application designated above (hereinafter the "Application"), I was an employee of Intel Corporation, the assignee of the Application.
2. I am a joint inventor of all claims of the present application.
3. Prior to the year 1999, I conceived the in the United States as evidenced by a copy of a signed invention disclosure form attached hereto as Exhibit I and diligently worked to constructively reduce the inventive sujbect matter to practice as evidenced by the filing of the Application for the claimed embodiments of the invention. I worked with a patent attorney as my other duties permitted in preparing the Application for filing with the United States Patent and Trademark Office. On information and belief, I received at least one draft of the Application for review and revision on or about May 4, 1999.
4. The dates redacted from Exhibit I are prior to the year 1999.
5. Other material redacted from Exhibit I is not related to dating the conception or reduction to practice of the inventive subject matter.

DECLARATION UNDER 37 C.F.R. § 1.131
Serial Number: 09/347,690
Filing Date: July 2, 1999
Title: LOGIC VERIFICATION IN LARGE SYSTEMS

6. Tom Tetzlaff was not an inventor of the inventive subject matter. Mr. Tetzlaff worked as an intern at Intel Corporation, and was directed to create programs which operated according to various embodiments of the invention after it was conceived. Mr. Tetzlaff worked as a programmer under the supervision of Honghua Yang and Jeremy Casas.

8. The patent application was filed on July 2, 1999.

9. The invention was completed by me as the co-inventor of the subject matter of claims under rejection.

10. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 11/25/02

Erik M. Seligman

Respectfully submitted,
MANPREET S. KHAIRA ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
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Date November 27, 2002 By Danny Padys
Danny J. Padys
Reg. No. 35,635

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 27 day of November, 2002.

Jane Sugers
Name

Signature

EXHIBIT I

REDACTED INVENTION DISCLOSURE FORM

INTEL CONFIDENTIAL

FOR ML IP COMMITTEE

(ML Comm)

INTEL INVENTION DISCLOSURE

MPG/DT/SCL

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to the Legal Department at JF3-147. If you have any questions, please call 264-0444 or 264-0998.

1.

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(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Simulation of Large Circuits on Intel Servers

3. What technology/product/process (code name) does it relate to: _ Circuit Logic Verification

4. Stage of development (i.e. % complete) 100%

5. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

NO: X YES: DATE WAS OR WILL BE PUBLISHED:

If YES, was the manuscript submitted for pre-publication approval? YES: NO:

(b) Has your invention been used/sold or planned to be used/sold by Intel or others? (In use at Intel)

NO: YES: X DATE WAS OR WILL BE SOLD: None

(c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?

NO: X YES: Name of SIG/Standard/Specification:

(d) If the invention is a semiconductor device, actual or anticipated date of tapeout?

(e) If the invention is software, actual or anticipated date of any beta tests. _ already in use

6. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia?

NO: X YES: Name of individual or entity:

PLEASE READ AND FOLLOW THE DIRECTIONS ON THE ATTACHED PAGE ON HOW TO WRITE A DESCRIPTION OF YOUR INVENTION

Please attach a page to this form, *DATED AND SIGNED BY AT LEAST ONE PERSON WHO* IS NOT A NAMED INVENTOR, to provide a description of the invention, and include the following information:

1. Describe in detail how the invention works.
2. Describe advantage(s) of your invention over what is done now.
3. Include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.
4. Value of your invention to Intel (how will it be used?).
5. Identify the closest or most pertinent prior art that you are aware of.
6. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

*HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM

[redacted] GREG SPIRAKIS [redacted]

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

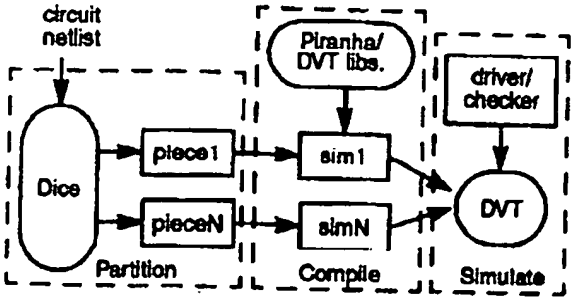
SIMULATION OF LARGE CIRCUITS ON INTEL SERVERS

Manpreet Khaira, Steve Otto, Honghua Hannah Yang, Mandar Joshi, Jeremy Casas, Erik Seligman

MS-JFT-104 {hyang, jcasas}@ichips.intel.com

INVENTION AND HOW IT WORKS

This disclosure describes a breakthrough technology, called Shark, that is the only known technique that allows the software simulation of 20+ million transistors. Shark presents a three-stage approach to simulating very large circuits as shown in the following diagram:



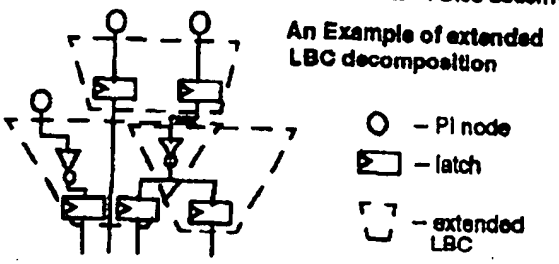
Shark first uses the Dice circuit partitioner to partition large circuits into smaller sub-circuits which are more manageable to build and simulate individually. Each sub-circuit or partition is then built as a stand-alone simulator using the Piranha simulator. Finally, DVT is used to run the different partitions, together with a test driver/checker, to form one large simulation of the entire circuit.

- The innovative partitioning approach in Dice enables Shark to scale to circuits with 20+ million devices, making it a solution for all future logic verification needs. It also enables scaling for performance. A simulation speed-up linear to the number of processors is achieved for up to 96 processors. Previous partitioners for parallel simulation had only limited success due to high communication overhead, load imbalance, and lack of capacity for handling full chip circuits.

- Dice partitioner has the use of a combination of several powerful activity weight functions in the load balance scheme. They cover all types of devices in micro-processor designs such as multiple clocks, and non-latch sequential elements.

NEW IDEAS IN SHARK

(1) A circuit partitioner based on a new idea called "extended Latch Boundary Component decomposition", or extended LBCs. The LBC concept by itself is not new. Innovation in our partitioner is to determine how to cluster the LBCs to form extended LBCs, so that the overall simulation speeds up. An extended LBC is a subcircuit that starts from latches and/or primary outputs and ends at latches and/or primary inputs. An extended LBC may contain internal latches and may overlap with another LBC. Dice decomposes a circuit into extended LBCs by traversing the circuit hierarchy and putting heavily correlated devices into the same extended LBC so as to reduce logic replication and reduce the final communication cost.



Our extended LBC formulation : only 2 communication steps are needed to evaluate the circuit every clock phase. We are also able to minimize circuit replication to about 10%, and communication cost to less than 10% of the total time.

(2) Once the extended LBCs are created, they partitioned into as many pieces as the number of processors being used. We have developed a new algorithm for partitioning the extended LBCs to allow for load balancing and overlap minimization. Load balancing is based on balancing a critical weight function of the number of latches, their activation during different clock phases, and the size of extended LBCs.

(3) In our observation, the load balancing obtained using the weight function defined in (2) is not very reliable. We invented a scheme for improving the load balance by a significant amount using activity data feedback. In this scheme, simulation speed data is collected by simulating subcircuits, and is normalized to form a weight function for each transistor in the circuit.

This scheme is independent of latches. In addition, it handles multiple clocks, since elements connecting to slow clocks have low activity. It also handles other sequential elements such as memory devices and state holders that are not latches.

(4) When simulating the network,

We use a broadcast-and-collect algorithm which *substantially improves performance* by removing the time to process data packets arriving.

(5) The Dice partitioner uses a data abstraction technique to form extended LBCs at the standard cell level, and then expands the standard cells to transistors after partitioning.

Technical Witness: TIMOTHY KAM

Timothy Kam

The Shark approach to solving switch-level circuit simulation makes it the solution for all future Intel logic verification (LVR) needs. It will save dollars by eliminating the need to purchase custom hardware accelerators

From a throughput perspective, Shark runs on standard workstations. This allows designers to do LVR on their designs whenever they want to and not wait in line on a few hardware accelerators as was done previously. This should help increase the quality of the processor (by running more tests due to availability of compute cycles) and at the same time increase the productivity of the designers by eliminating wait-time on LVR runs.

Currently, Shark is the tool-of-choice for performing LVR of current processor design groups and will most likely be used by all future processor design groups. It is also being evaluated by other chip design teams . In fact, we don't expect to be buying any more hardware accelerators for logic verification.